CLAIMS

What is claimed is:

1. An apparatus comprising:

core control logic to provide a data signal; and

output drive logic including a local data latch and a transmitter, the data latch to receive the data signal and to provide true and complementary forms of the data signal to the transmitter over symmetrical signal paths, the transmitter to provide an output signal to an external receiver.

2. The apparatus of claim 1 wherein true and complementary signal paths between the local data latch and the transmitter are symmetrical.

3. The apparatus of claim 1 further comprising

design for testability (DFT) logic local to the transmitter, the DFT logic including an internal receiver coupled to an output of the transmitter and a local DFT latch coupled to an output of the internal receiver.

4. The apparatus of claim 3 wherein the internal receiver comprises a dual oxide sense amplifier.

5. The apparatus of claim 4 wherein the dual oxide sense amplifier includes precharge logic to precharge input lines to the dual oxide sense amplifier to a first voltage level.

6. The apparatus of claim 5 wherein the dual oxide sense amplifier is clocked.

7. The apparatus of claim 5 wherein the dual oxide sense amplifier is capable of operating in response to low voltage swing, differential input signals.

8. A video controller comprising:

a video control core to provide video control and data signals;

a data transmission output driver including a data latch and a transmitter, the data latch to latch data from the video control core destined for the transmitter, the transmitter to be coupled to a receiver; and

design for testability (DFT) logic including an internal receiver and a local DFT latch, the internal receiver to compare an output of the transmitter with a reference voltage, the local DFT latch to latch a result of the comparison.

9. The video controller of claim 8 wherein

true and complementary signal paths between the data latch and the transmitter are symmetrical.

10. The video controller of claim 8 wherein the internal receiver comprises two dual oxide sense amplifiers, a first dual oxide sense amplifier to

receive a true form of the transmitter output, a second dual oxide sense amplifier to receive a complementary form of the transmitter output.

11. The video controller of claim 10 wherein signal lines of the dual oxide sense amplifiers are precharged prior to sensing.

12. The video controller of claim 11 wherein the dual oxide sense amplifiers receive two different, non-ground supply voltages.

13. A mobile computer system comprising:

a battery to power the computer system in the absence of an alternate power connection;

a processor to process instructions;

a memory coupled to the processor;

a memory controller coupled to the memory and the processor; and

a video controller coupled to the memory controller and to be coupled to an external display, the video controller comprising

core control logic to provide a video data signal; and

output drive logic including a local data latch and a transmitter, the data latch to receive the video data signal and to provide true and complementary forms of the data signal to the transmitter over symmetrical signal paths, the transmitter to provide an output signal to an external receiver.

14. The system of claim 13 wherein the video controller further comprises design for testability (DFT) logic local to the transmitter, the DFT logic including an internal receiver to receive an output signal from the transmitter and a local DFT latch to latch an output of the internal receiver.

15. The system of claim 14 wherein the internal receiver comprises a dual oxide sense amplifier that is also coupled to receive a reference voltage, the dual oxide sense amplifier to precharge input bit lines prior to sensing.

16. The system of claim 15 wherein the dual oxide sense amplifier is capable of sensing low voltage swing, differential signals.

17. A sense amplifier comprising:

a sensing circuit having differential input bit lines, the sensing circuit to sense a low voltage swing signal in response to an enable signal;

a precharge circuit to precharge the input bit lines; and

a high voltage conversion circuit to receive an input signal having a first voltage swing and to provide the enable signal having a larger voltage swing,

the sense amplifier including at least a first transistor having a gate oxide of a first thickness and a second transistor having a gate oxide of a second thickness greater than the first thickness.

18. The sense amplifier of claim 17 wherein the sense amplifier is clocked.

19. The sense amplifier of claim 17 wherein the sensing circuit includes an enable control gate having a gate oxide of the second thickness, the enable control gate being responsive to the enable signal to enable and disable the sensing circuit.

20. The sense amplifier of claim 19 wherein the sensing circuit includes a true data gate to receive a true form of input data over a first input bit line and a complementary data gate to receive a complementary form of the input data over a second input bit line, the true and complementary data gates each having gate oxides of the second thickness.

21. A method comprising:

receiving video data from a video control core at a latch;

transmitting true and complementary forms of the video data from the latch to a local transmitter over symmetrical signal paths; and

providing output video data from the transmitter.

22. The method of claim 22 further comprising:

receiving the output data from the transmitter at an internal receiver;

comparing the output data to a reference signal;

locally latching an output of the internal receiver;

converting the output of the internal receiver; and

providing the converted output of the internal receiver to the video control core.

23. A method comprising:

precharging input bit lines of a sense amplifier to a first voltage level;

receiving a low voltage enable control signal;

converting the low voltage enable control signal to a higher voltage enable signal;

sensing low swing data signals on the input bit lines in response to a clock signal and the enable signal with a circuit that includes at least a first transistor having a first gate oxide thickness and at least a second transistor having a second gate oxide thickness thicker than the first gate oxide thickness.

24. The method of claim 23 further comprising:

disabling sensing in response to deasserting the enable signal.

25. A method comprising:

providing a video control core; and

providing a data transmission path including a transmitter and a local data latch, the local data latch to latch data from the video control core that is destined

for the transmitter and to provide true and complementary forms of the latched data to the transmitter over symmetrical signal paths.

26. The method of claim 25 further comprising:

providing a design for testability (DFT) path including an internal receiver to receive output data from the transmitter and a local DFT latch to latch output data from the internal receiver.

27. The method of claim 26 wherein providing a design for testability path includes providing an internal receiver comprising a dual oxide sense amplifier.

28. A method comprising:

providing a sensing circuit to sense low voltage swing differential input signals received over input bit lines;

providing a precharge circuit to precharge the input bit lines; and

providing a high voltage conversion circuit to convert an input enable control signal to a higher voltage enable signal to control the sensing circuit,

wherein providing the sensing circuit includes providing at least a first transistor having a first gate oxide thickness and at least a second transistor having a second gate oxide thickness thicker than the first gate oxide thickness.

29. The method of claim 28 wherein providing the sensing circuit includes providing the sensing circuit that is responsive to a clock signal to sense low voltage swing, differential input signals.